Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **D2**
2. **NC**
3. **D1**
4. **S1**
5. **S4**
6. **D4**
7. **NC**
8. **D3**
9. **S3**
10. **NC**
11. **V+**
12. **VL**
13. **VR**
14. **V-**
15. **A**
16. **S2**

**.081”**

**1 16 15**

**14**

**13**

**12**

**11**

**3**

**4**

**5**

**6**

**8 9 10**

**HI**

**5046**

**MASK**

**REF**

**.096”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: FLOATING**

**Mask Ref: HI 5046**

**APPROVED BY: DK DIE SIZE .081” X .096” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HI0-5046A**

**DG 10.1.2**

#### Rev B, 7/1